IN THE CLAIMS

Please amend the claims as follows.

1.-10. (Cancelled)

11. (Currently Amended) A semiconductor die comprising:

a substrate having a first planar surface having a first region with active circuitry including at least one of a transistor, resistor and a signal conductor thereon surrounded by an unused blank second region;

a second planar surface opposite the first planar surface;

one or more planar perimeter side surfaces in the second region, each planar perimeter side surface extending from the first planar surface to the second planar surface; and

each planar perimeter side surface of the semiconductor die being a flat surface substantially perpendicular to the first planar surface, with a top portion of each individual planar perimeter side surface disposed in the second region and within 5 microns of an edge of active circuitry in the first region.

12. (Original) The semiconductor die as recited in claim 11, wherein each planar perimeter side surface is transverse to the first planar surface and the second planar surface.

13. (Original) The semiconductor die as recited in claim 11, wherein the semiconductor die has a substantially rectangular shape.

14. (Original) The semiconductor die as recited in claim 11, wherein each planar perimeter surface is a ground surface.

15. (Currently Amended) A semiconductor die comprising:

a substrate having a first planar surface having a first region with active circuitry including at least one of a transistor, resistor and a signal conductor thereon surrounded by an unused blank second region;

a second planar surface opposite the first planar surface;

one or more planar perimeter side surfaces entirely contained in the second region, having a surface substantially perpendicular to the first planar surface, with a top portion of each individual planar perimeter side surface disposed in the second region and within 5 microns of an edge of active circuitry in the first region.

16. (Original) The semiconductor die as recited in claim 15, wherein each planar perimeter side surface is transverse to the first planar surface and the second planar surface.

17. (Original) The semiconductor die as recited in claim 15, wherein each planar perimeter side surface comprises a polished surface.

18. - 43. (Cancelled)